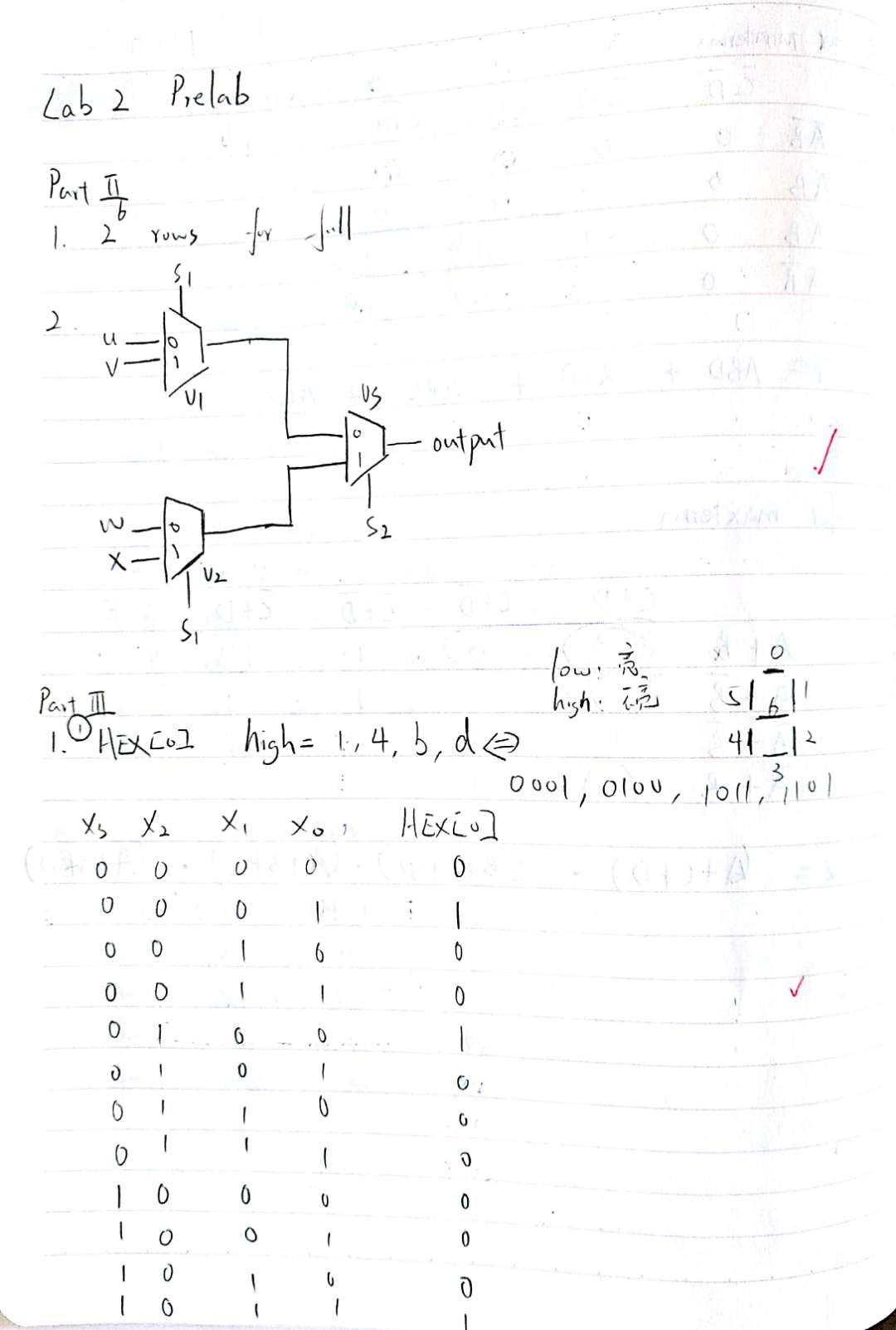
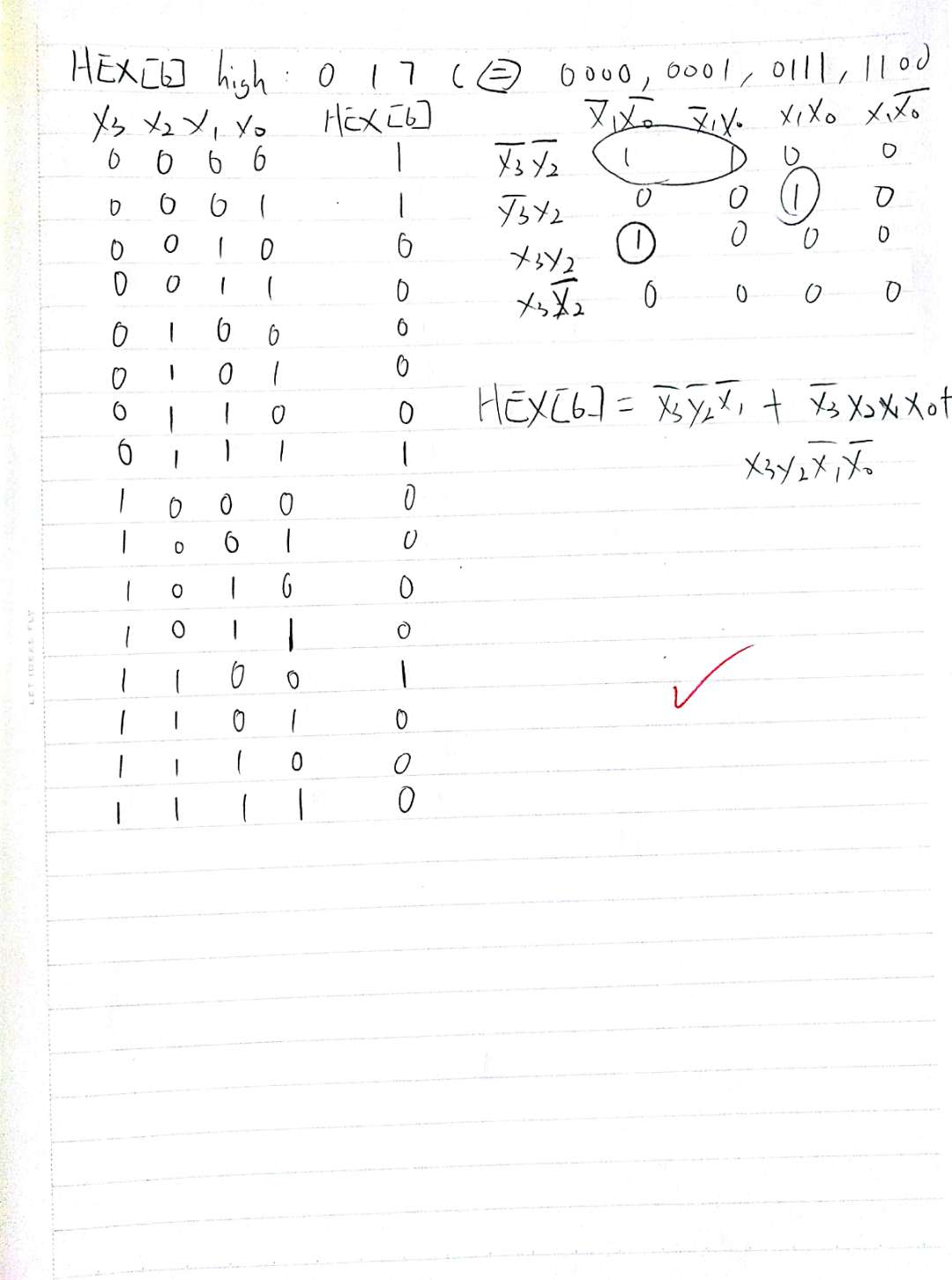
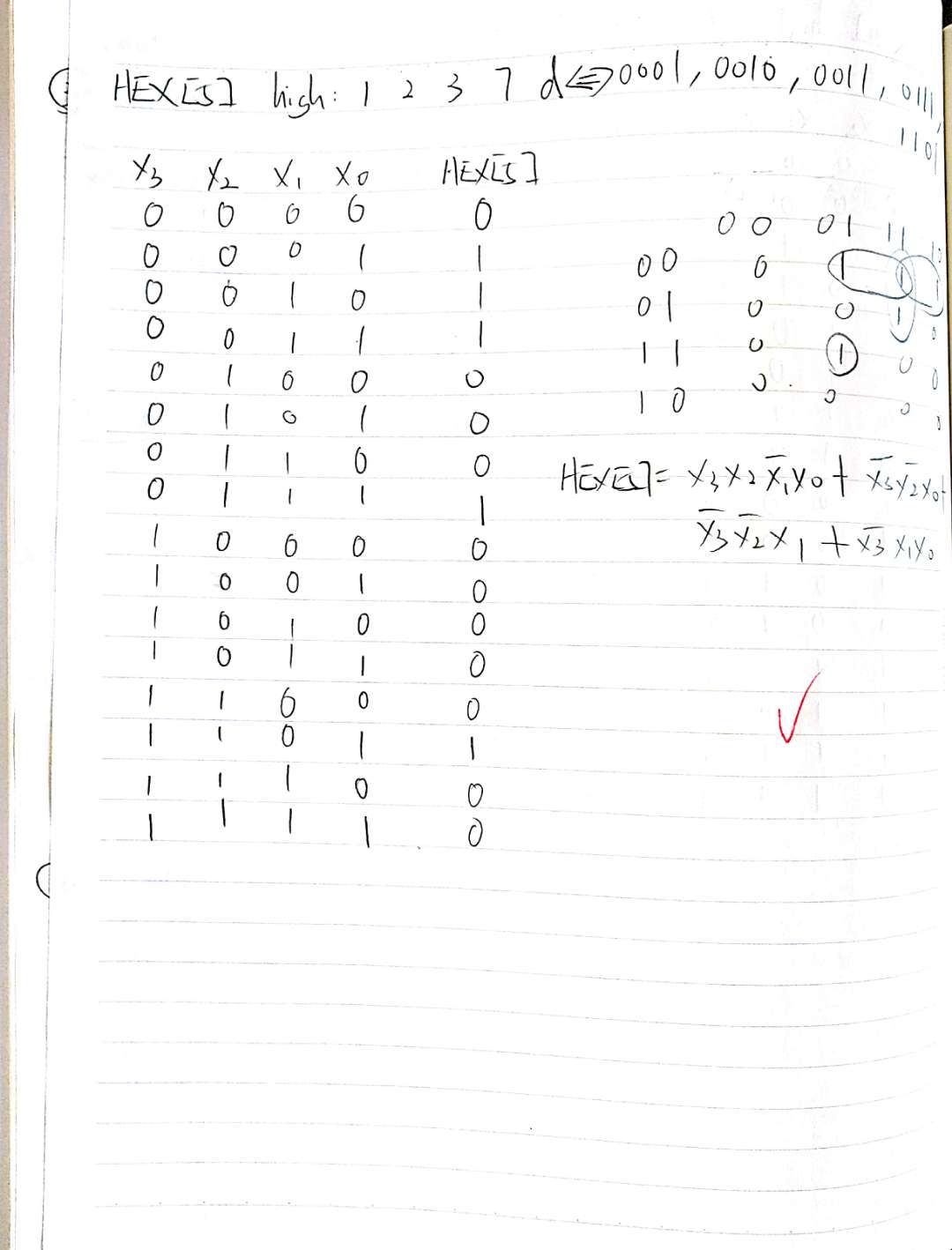
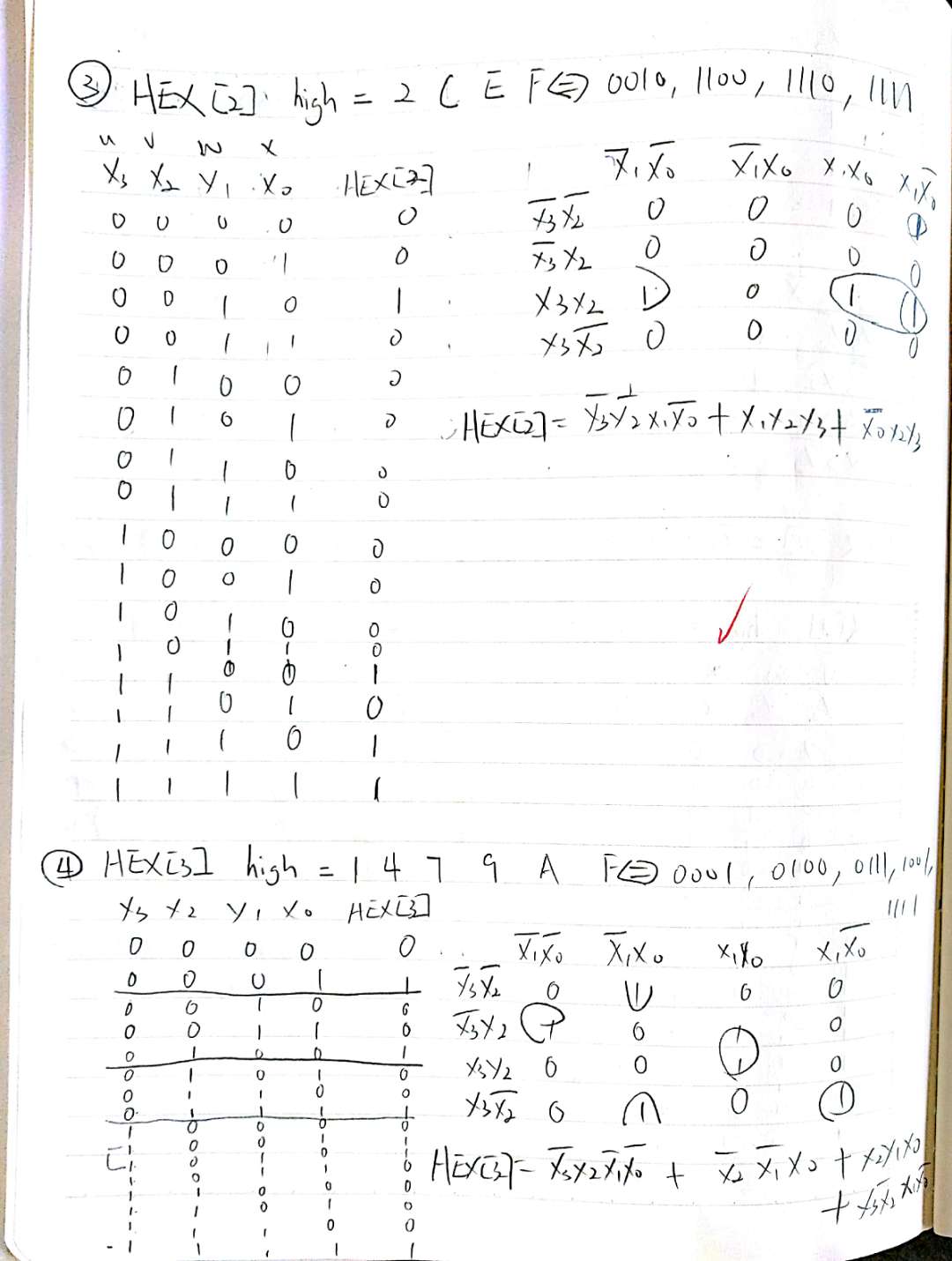
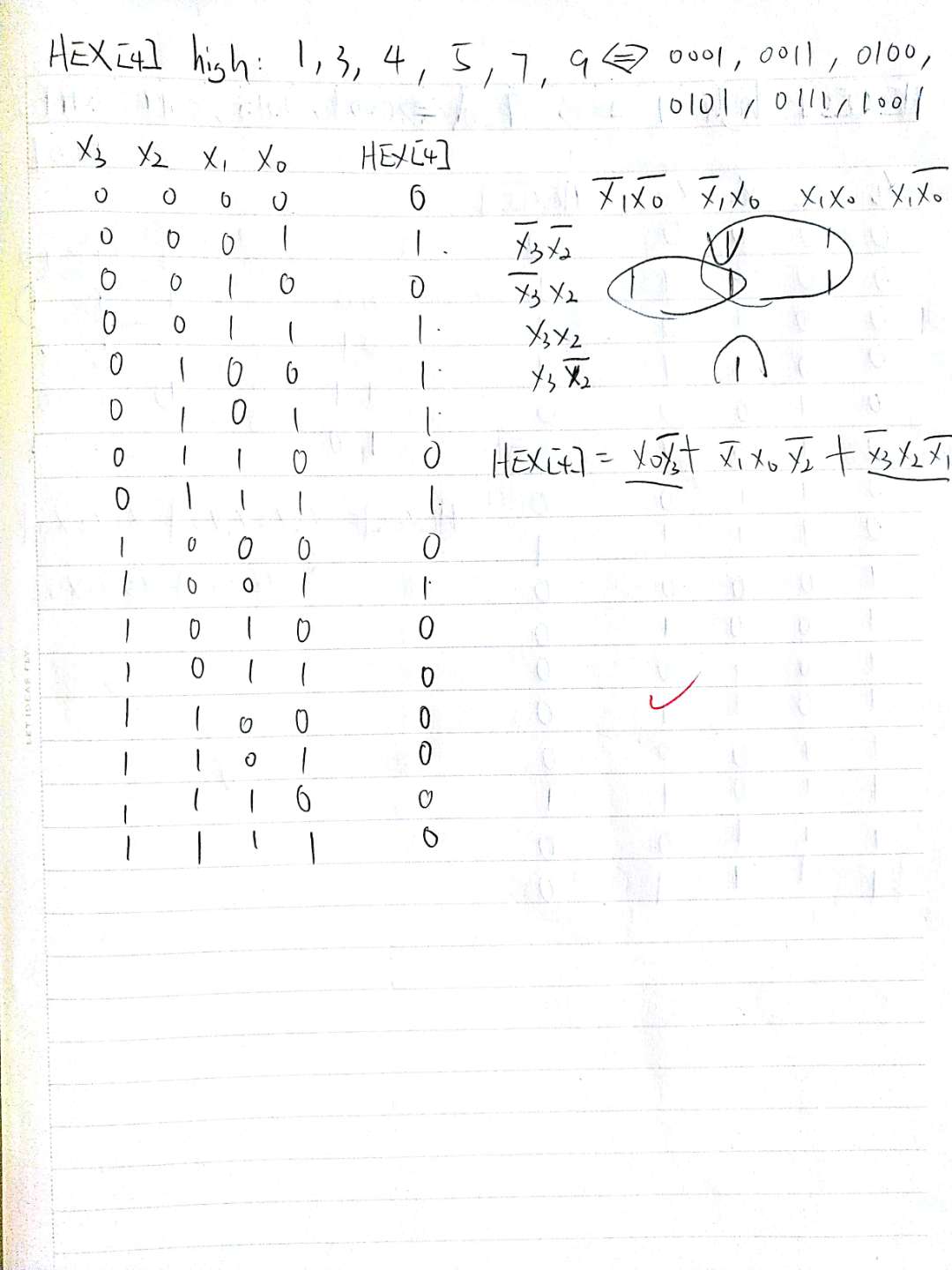
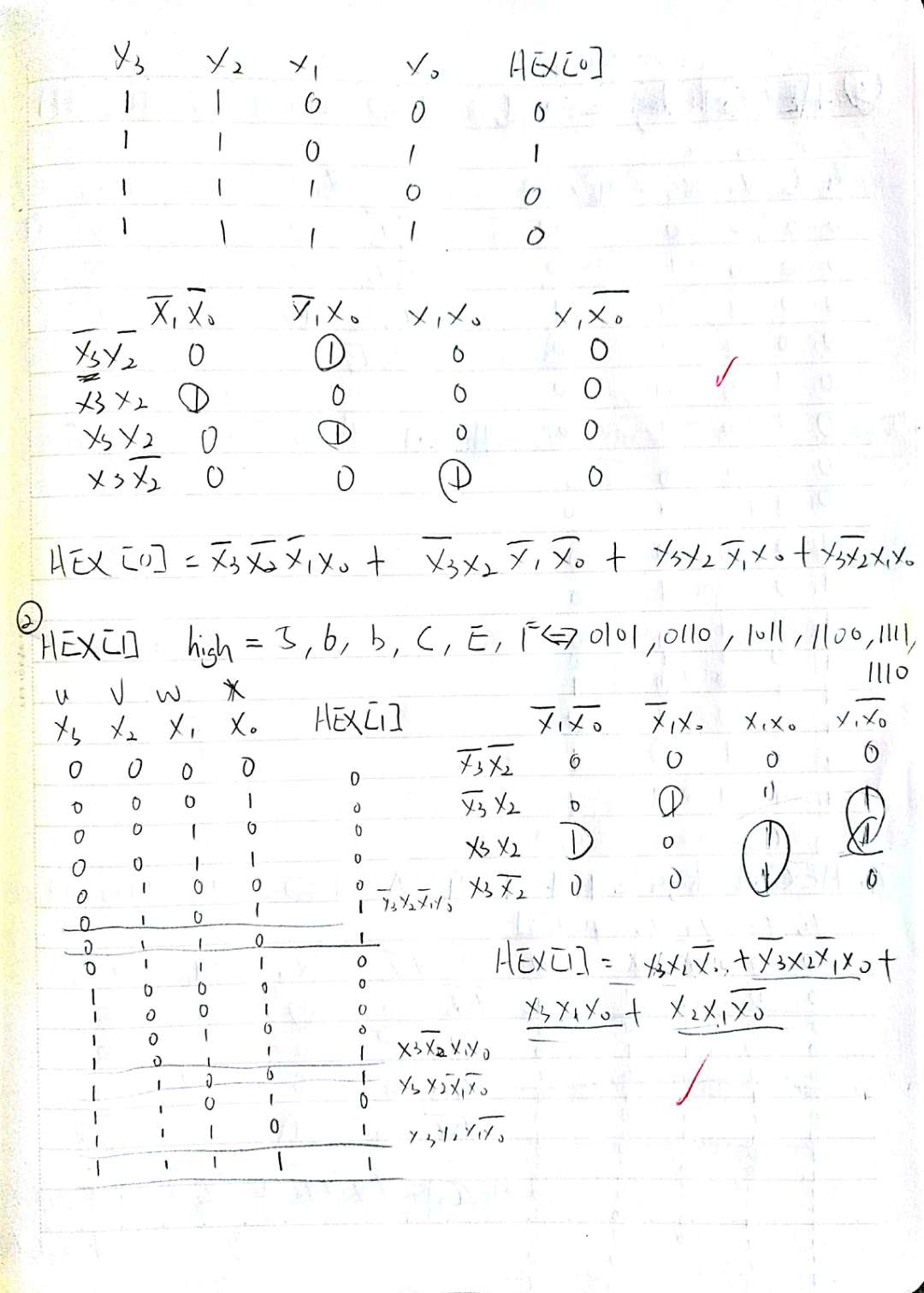
CSC258 Lab#2

Xin Luo/ Ruijie Sun 1003069706/

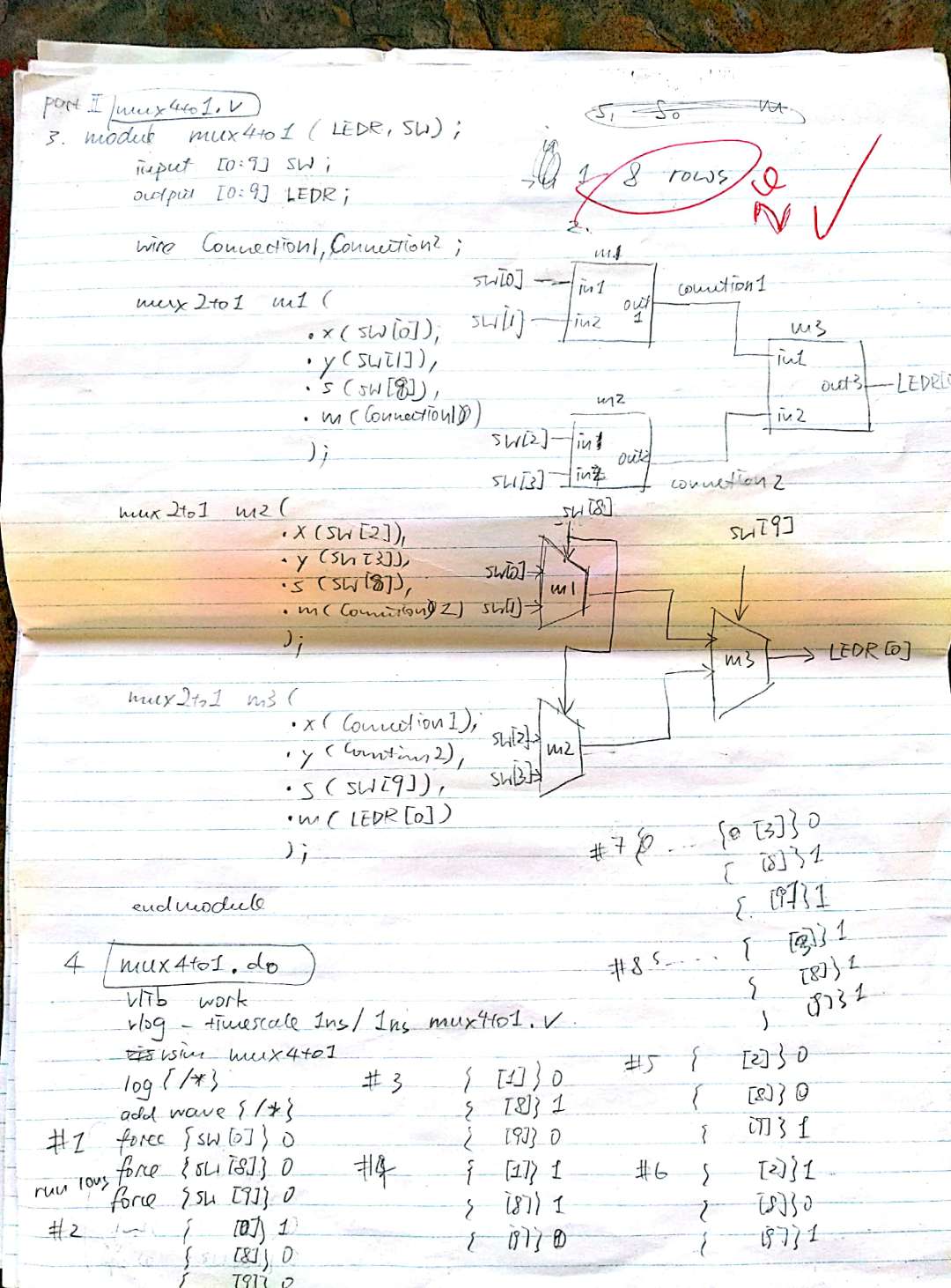
Part A (pre-lab)

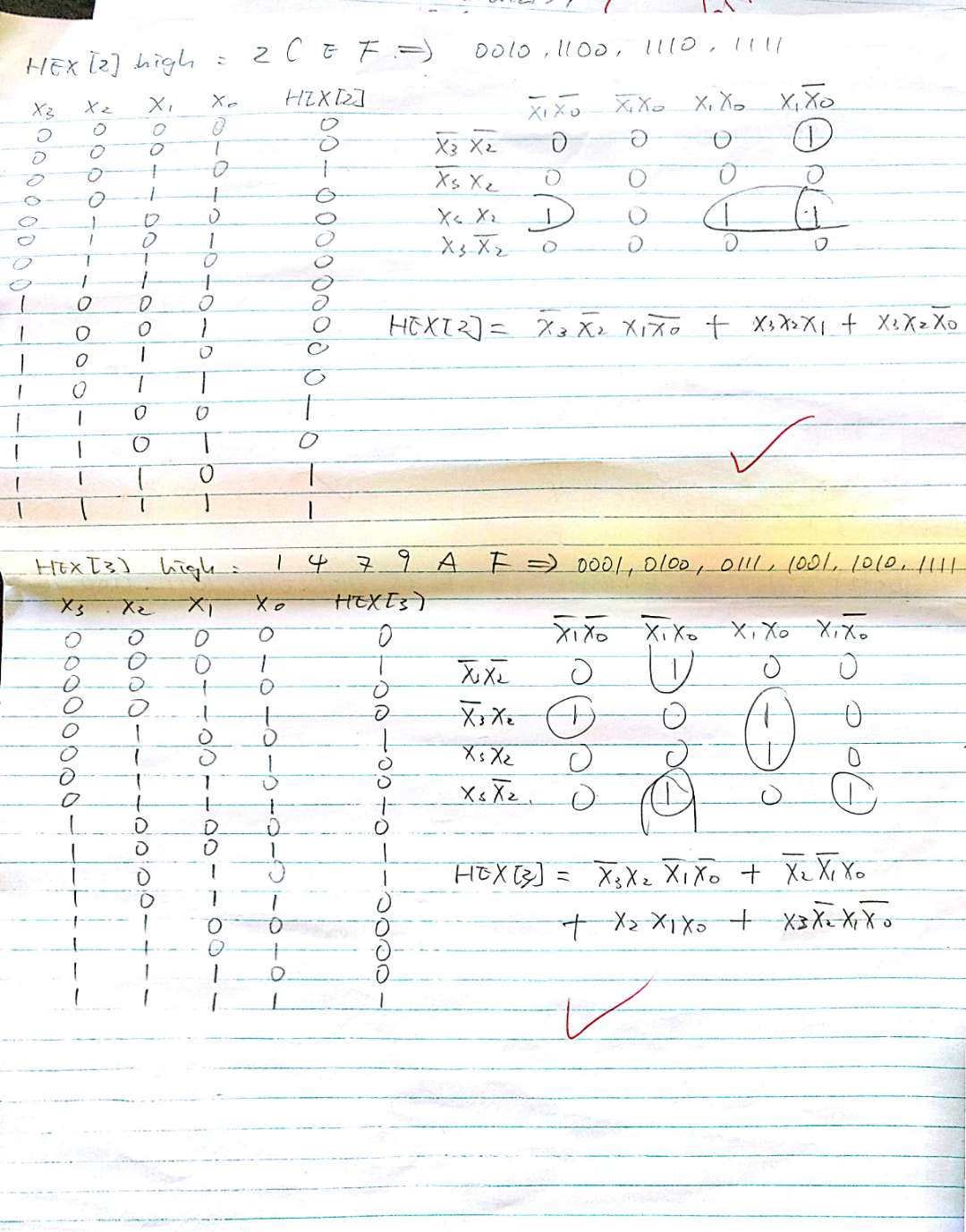
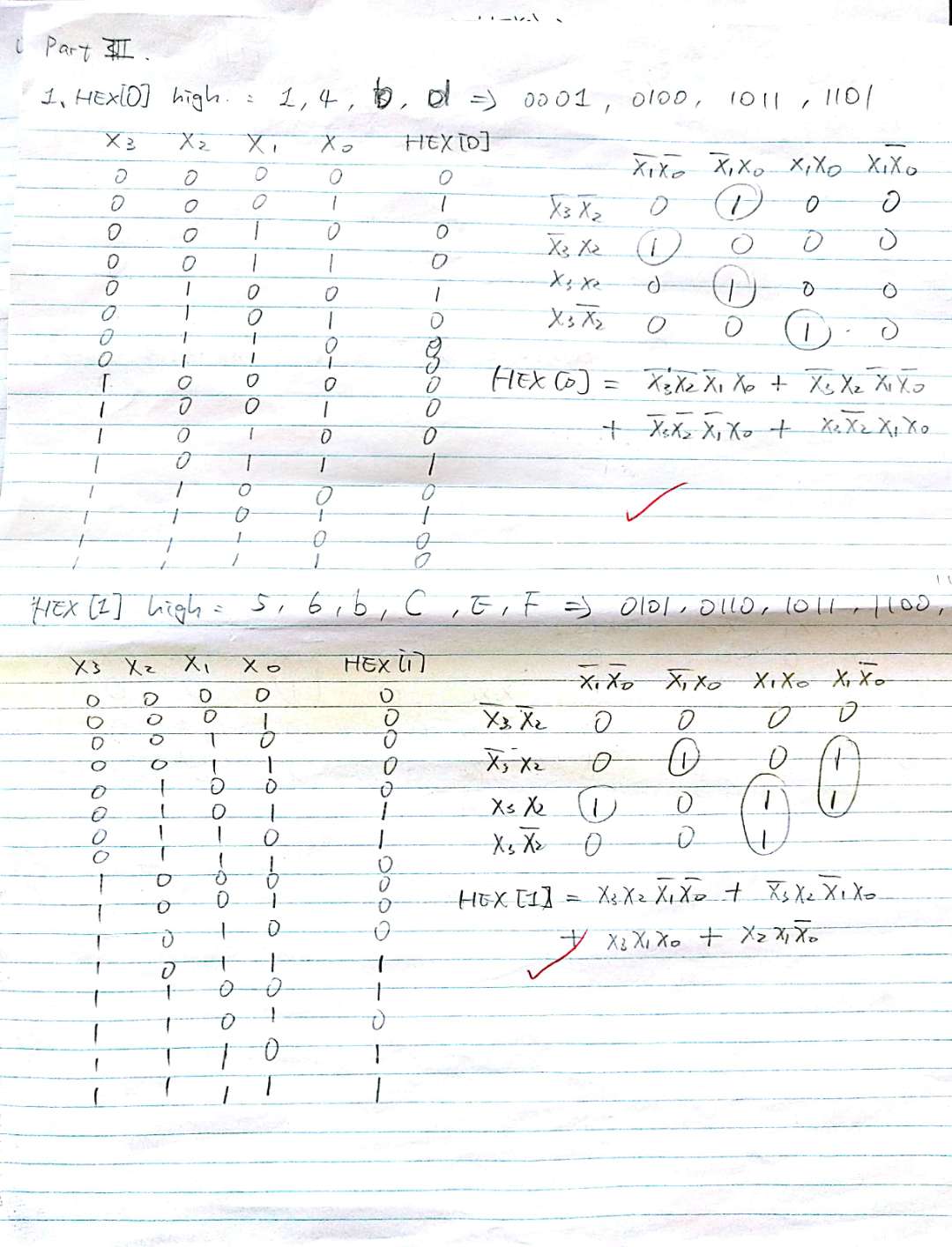
Ruijie Sun:

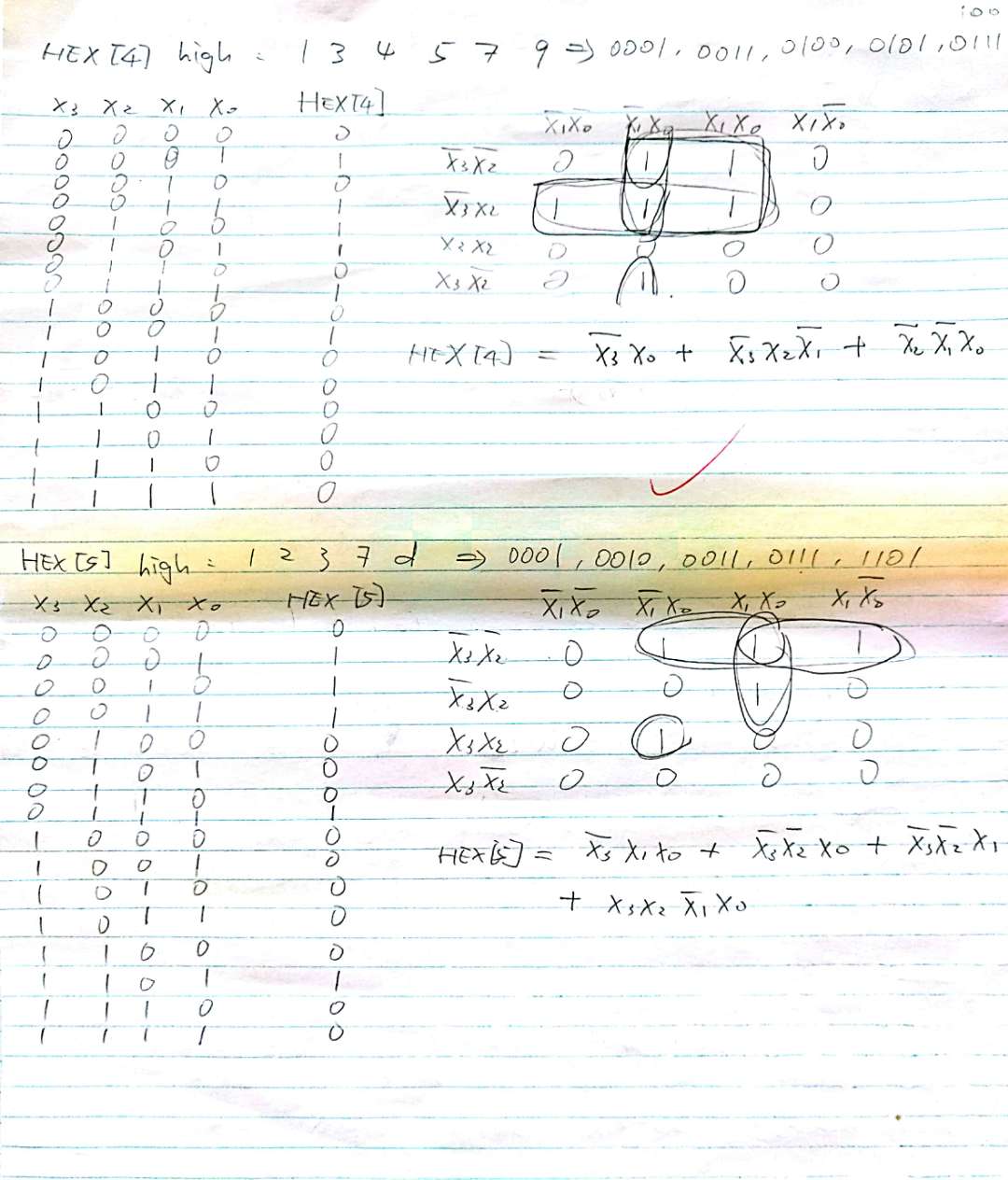


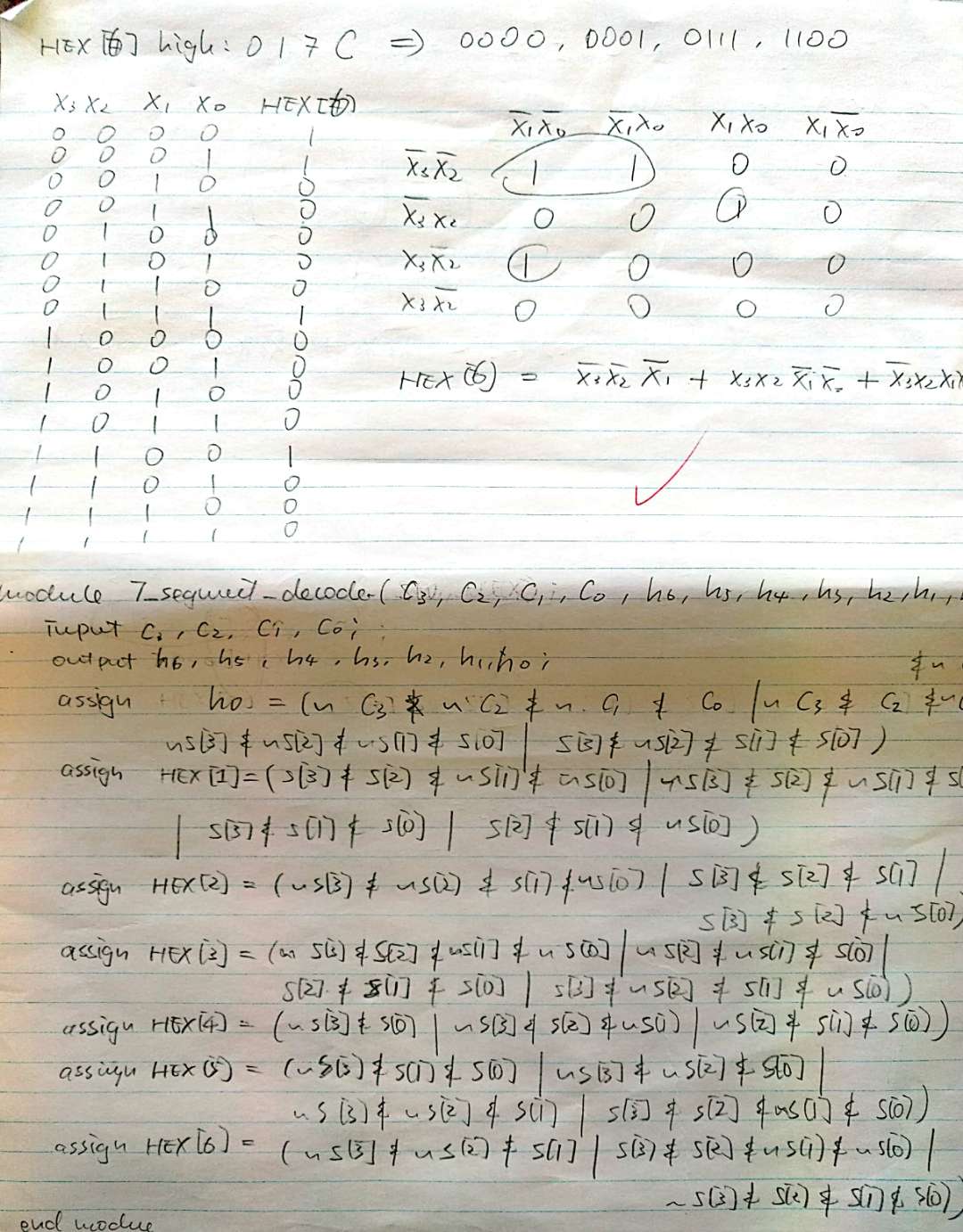


Xin Luo:



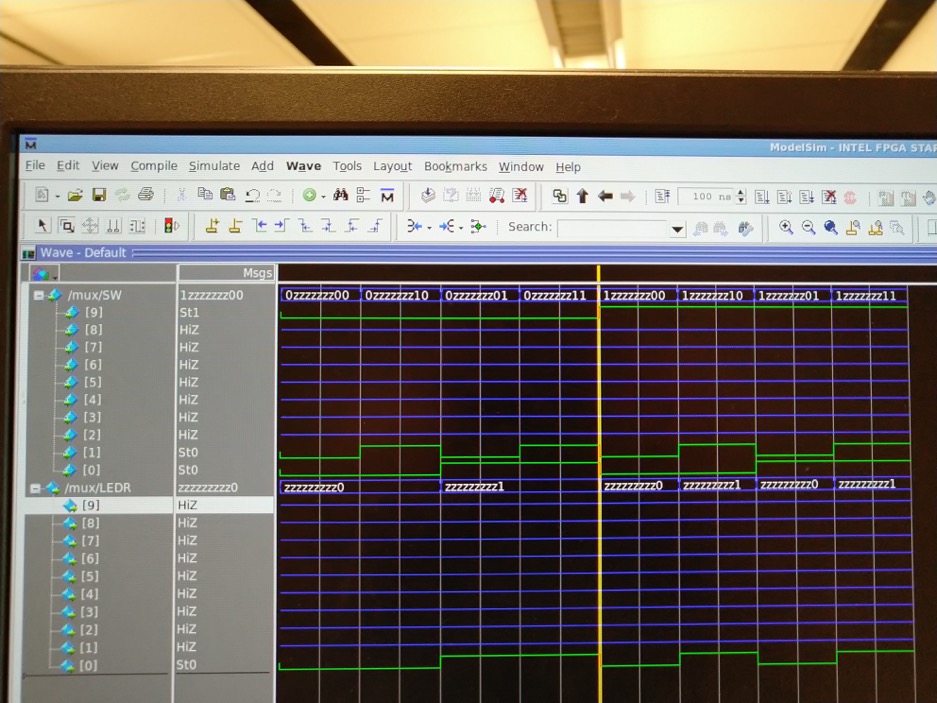




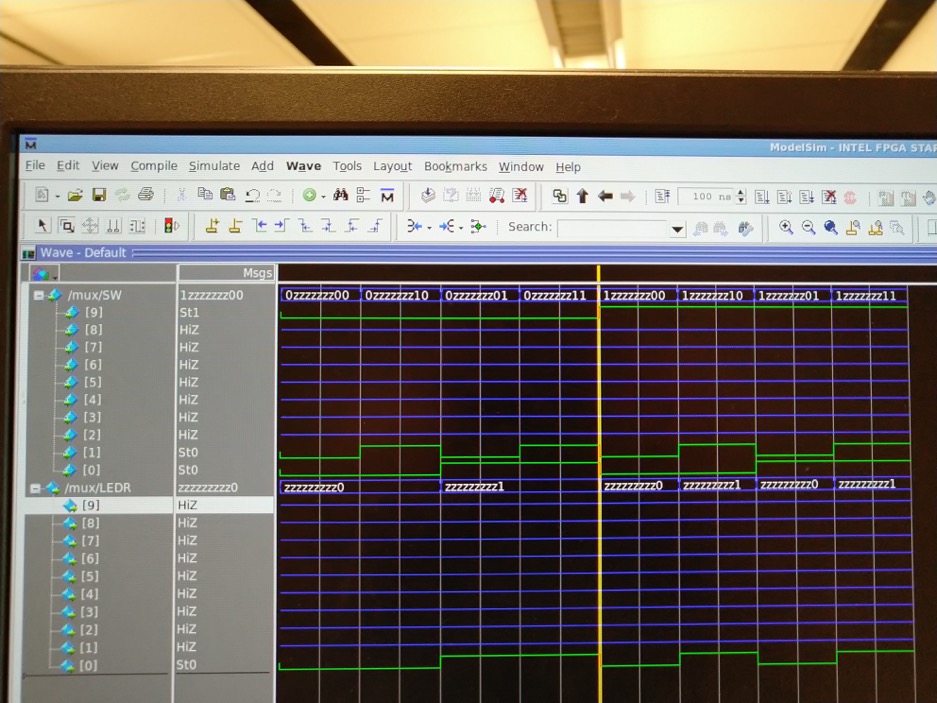


Part B (simulation for part1):

Ruijie Sun:



Xin Luo:



Short answer 3:

The output on the FPGA chip matches the the simulation .

Short answer 4:

The time we need to compile the verilog file and test the results on the FPGA chip is much longer then we directly simulate the result on the ModelSim using .do file.

Part C (Verilog code for Part2)

Ruijie Sun:

module mux4to1(u,v,w,x,s1,s2,m);

input u; //selected when s1 is 0 and s2 is 0

input v; //selected when s1 is 0 and s2 is 1

input w; //selected when s1 is 1 and s2 is 0

input x; //selected when s1 is 1 and s2 is 1

input s1; //select signal # 1

input s2; //select signal # 2

wire A;

wire B;

output m; //output

mux2to1 m1(

.x(u),

.y(v),

.s(s1),

.m(A)

);

mux2to1 m2(

.x(w),

.y(x),

.s(s1),

.m(B)

);

mux2to1 m3(

.x(A),

.y(B),

.s(s2),

.m(m)

);

endmodule

module mux2to1(x, y, s, m);

input x; //selected when s is 0

input y; //selected when s is 1

input s; //select signal

output m; //output

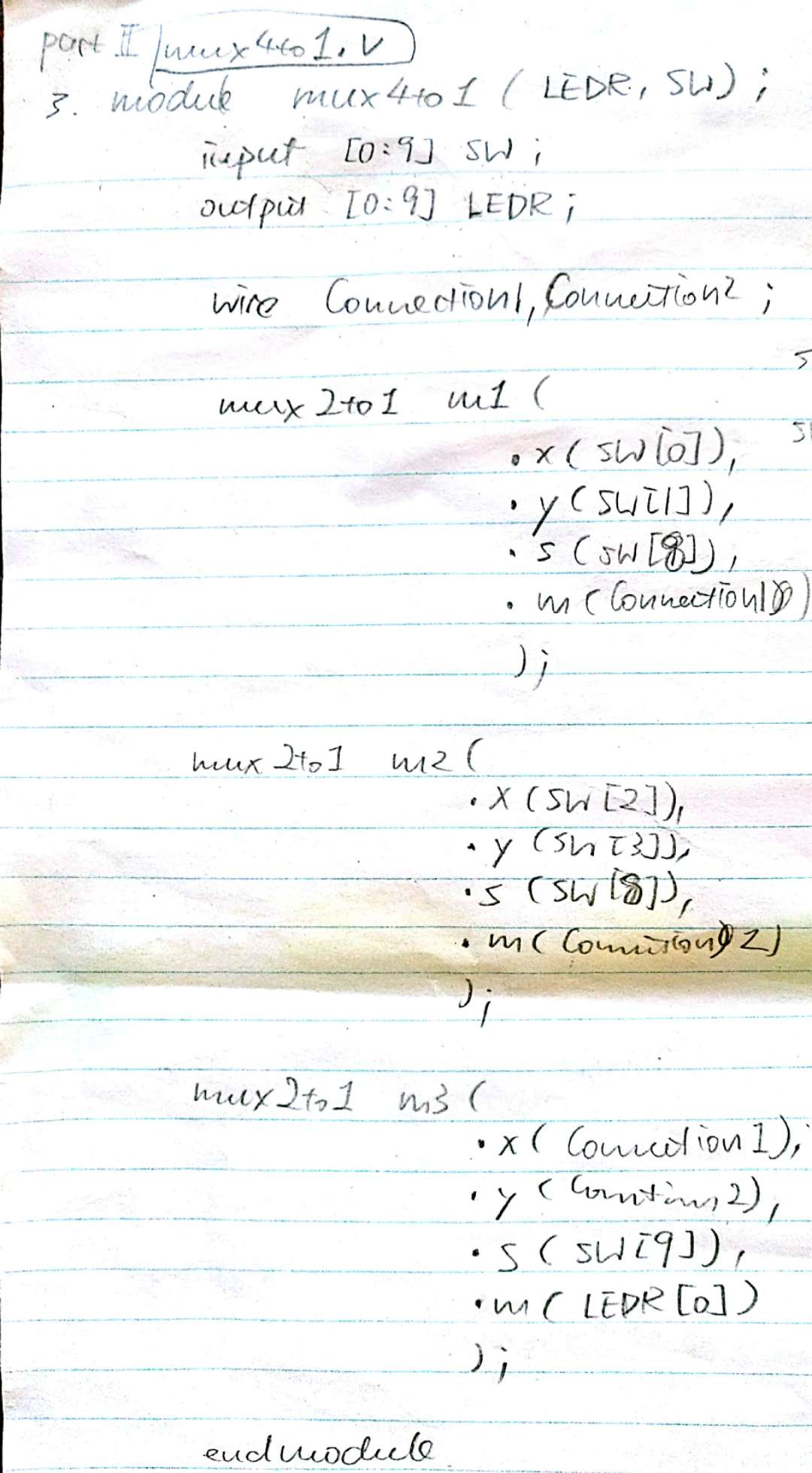
assign m = s & y | ~s & x;

// OR

// assign m = s ? y : x;

endmodule

Xin Luo:



PartD: (Verilog code for part3):

Ruijie Sun:

module decoder(HEX0, SW);

input [9:0] SW;

output [6:0] HEX0;

decoderr u0(

.u(SW[0]),

.v(SW[1]),

.w(SW[2]),

.x(SW[3]),

.HEX00(HEX0[0]),

.HEX01(HEX0[1]),

.HEX02(HEX0[2]),

.HEX03(HEX0[3]),

.HEX04(HEX0[4]),

.HEX05(HEX0[5]),

.HEX06(HEX0[6])

);

endmodule

module decoderr(u,v,w,x,HEX00,HEX01,HEX02,HEX03,HEX04,HEX05,HEX06);

input u;

input v;

input w;

input x;

output HEX00;

output HEX01;

output HEX02;

output HEX03;

output HEX04;

output HEX05;

output HEX06;

assign HEX00 = ~u & ~v & ~w &x | ~u & v & ~w & ~x| u & ~v & w & x | u & v & ~w & x ;

assign HEX01 = ~u & v & ~w & x | u & w & x | u & v & ~x | v & w & ~x ;

assign HEX02 = u & v & ~x | ~v & w & ~x;

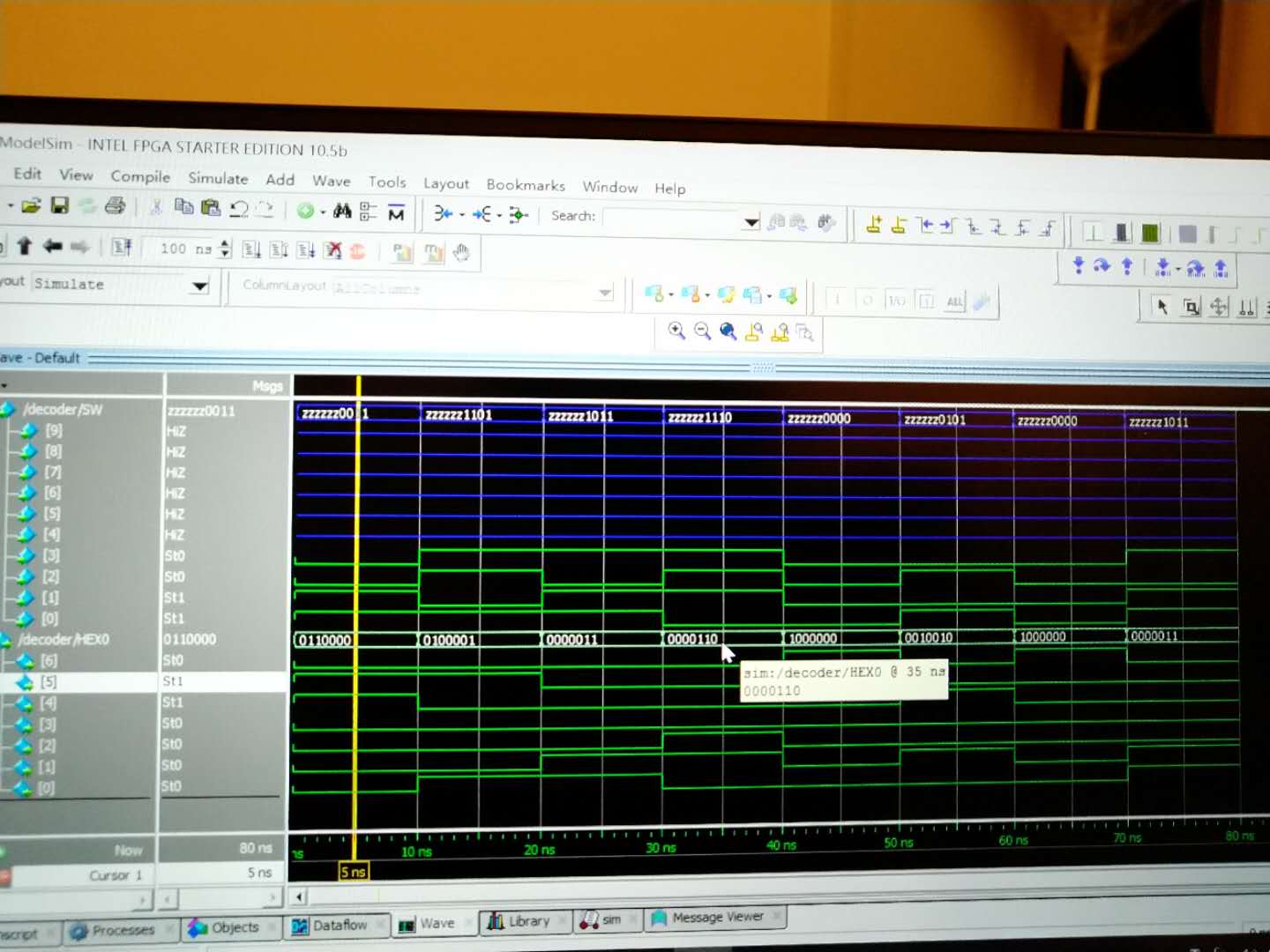
assign HEX03 = ~u & v & ~w & ~x | ~v & ~w & x | v & w & x | u & ~v & w & ~x ;

assign HEX04 = ~u & v & ~w | ~v & ~w & x | ~u & x ;

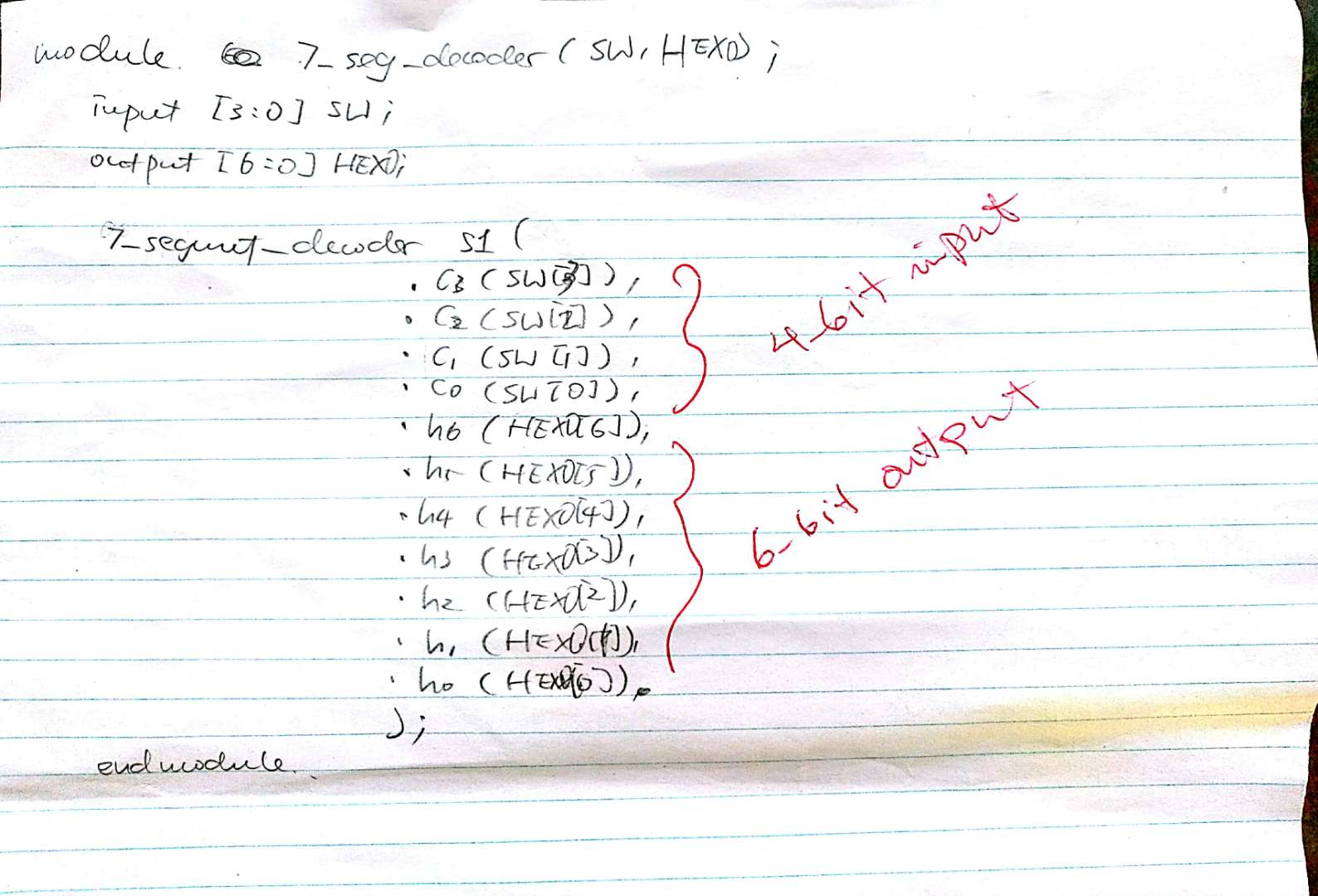
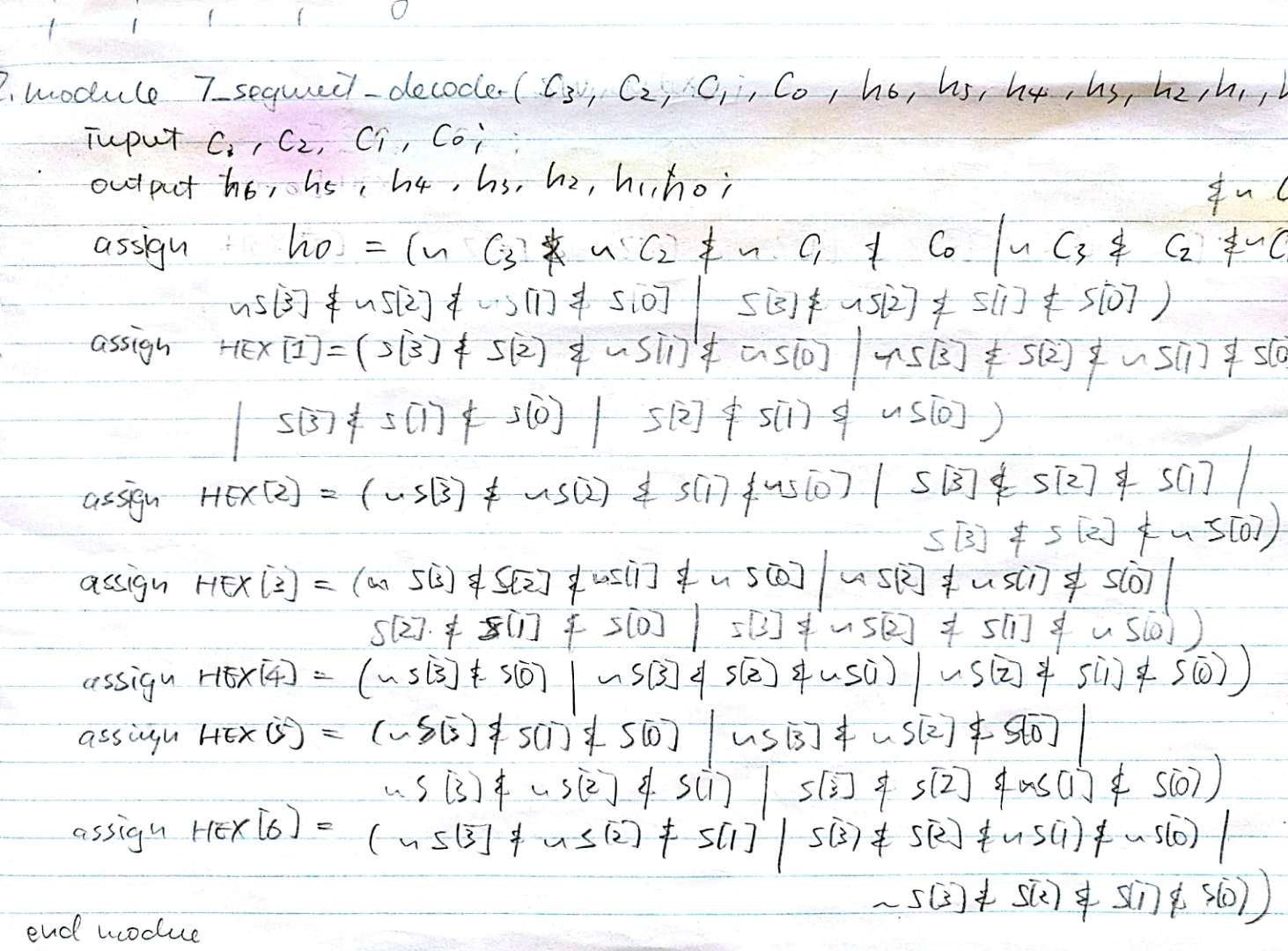
assign HEX05 = ~u & ~v & x | ~u & ~v & w | ~u & w & x | u & v & ~w & x ;

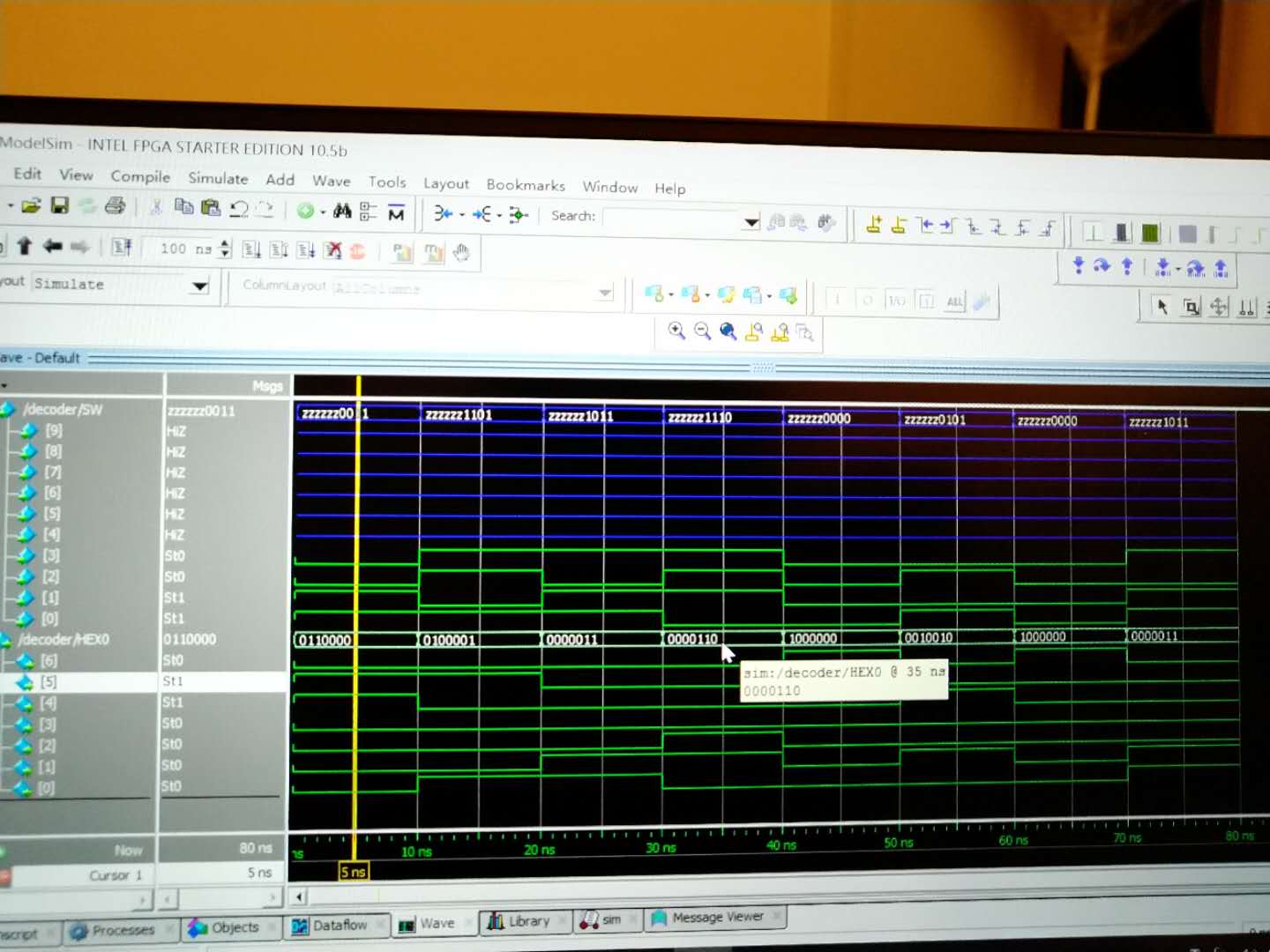
assign HEX06 = ~u & ~v & ~w | ~u & v & w & x | u & v & ~w & ~x ;

endmodule



Xin Luo:





Part E:

1. We can be familiar with the process of handling the FPGA chip and understand how the circuit work.
2. The most interesting part of this lab is to do it by our self instead of learn from book.
3. If there can be more TAs in the lab to check our work, the lab time will be much shorter because most people finish their work but TA don’t have time to check, we always need to wait for a longer time than we actually need.